AND8237/D

Low $V_{CE(sat)}$ BJT in 1206A ChipFET™ Package Recommended Pad Pattern and Thermal Performance

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APPLICATION NOTE

INTRODUCTION

ON Semiconductor ChipFETs in the leadless 1206A package, which features the same outline as popular 1206A resistors and capacitors, provides all the performance of a true power semiconductor device. The 1206A ChipFET has a smaller footprint than the popular TSOP−6 (SOT23−6), but its thermal performance bears comparison with the much larger SO−8. This technical note discusses the ChipFET 1206A pinout, package outline, pad patterns, evaluation board layout and thermal performance.

Pinout

Figure 1 shows the pinout description and Pin 1 identification for the 1206A ChipFET device. The pinout is similar to the TSOP−6 configuration, with two additional collector pins to enhance power dissipation and thermal performance. The legs of the device are very short, again helping to reduce the thermal path to the external heatsink/ PCB and allowing a larger die to be fitted in the device.

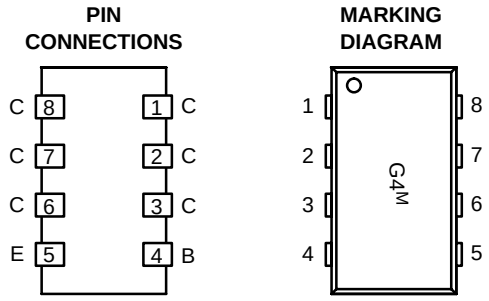

Figure 1.

Basic Pad Patterns

The basic pad layout with dimensions is shown in Figure 2. This is sufficient for low $V_{CE(sat)}$ BJT applications, but power semiconductor performance requires a greater copper pad area, particularly for the collector leads. The minimum recommended pad pattern, shown in Figure 3, improves the thermal area of the collector connections (Pins 1, 2, 3, 6, 7, 8) while remaining within the confines of the basic footprint. The collector copper area is 0.0054 sq. in. or 3.51 sq. mm. This will assist the power dissipation away from the device (through the copper lead−frame) and into the board and exterior chassis (if applicable) for the device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further. An example of this method is implemented on the Evaluation Board described in the next section (Figure 4).

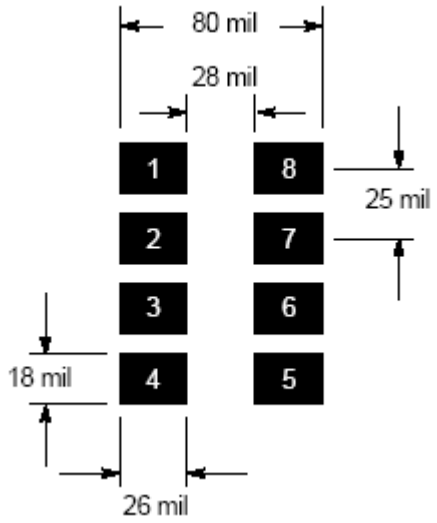

Figure 2. Basic Pad Layout

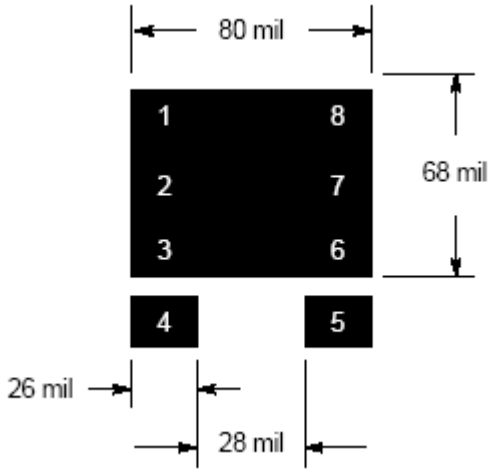

Figure 3. Minimum Recommended Pad Pattern

Evaluation Board for the 1206A

The ChipFET 1206A evaluation board measures 0.6 in by 0.5 in. Its copper pad pattern consists of an increased pad area around the six collector leads on the top−side − approximately 0.0482 sq. in. 31.1 sq. mm − and vias added through to the underside of the board, again with a maximized copper pad area of approximately the board−size dimensions. The outer package outline is for the 8−pin DIP, which will allow test sockets to be used to assist in testing.

The thermal performance of the 1206A on this board has been measured with the results following on the next page. The testing included comparison with the minimum recommended footprint on the evaluation board−size PCB and the industry standard one−inch square FR4 PCB with copper on both sides of the board.

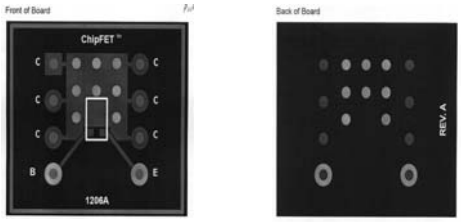

Figure 4. Evaluation Board

Thermal Performance

Junction−to−Foot Thermal Resistance (Package Performance)

Thermal performance for the 1206A ChipFET measured as junction−to−foot thermal resistance is 15°C/W typical, 20°C/W maximum for the device. The “foot” is the collector lead of the device as it connects with the body. This is identical to the SO−8 package $R_{\theta JF}$ performance, a feat made possible by shortening the leads to the point where they become only a small part of the total footprint area.

Junction−to−Ambient Thermal Resistance (Dependent on PCB Size)

The $R_{\theta JA}$ typical for the 1206A ChipFET is 80°C/W steady state, compared with 68°C/W for the SO−8. Maximum ratings are 95°C/W for the 1206−8 versus 80°C/W for the SO−8.

Testing

To aid comparison further, Figure 5 illustrates ChipFET 1206A thermal performance on two different board sizes and three different pad patterns. The results display the thermal performance out to steady state and produce a graphic account of how an increased copper pad area for the collector connections can enhance thermal performance. The measured steady state values of $R_{\theta JA}$ for the 1206A ChipFET are:

- Minimum recommended pad pattern (see Figure 3) on the evaluation board size of 0.5 in. x 0.6 in. = 156°C/W
- The evaluation board with the pad pattern described in Figure 4 = 111°C/W
- Industry standard one, square PCB with maximum copper both sides = 78°C/W

The results show that a major reduction can be made in the thermal resistance by increasing the copper collector area. In this example, a 45°C/W reduction was achieved without having to increase the size of the board. If increasing board size is an option, a further 33°C/W reduction was obtained by maximizing the copper from the collector on the larger 1″ square PCB.

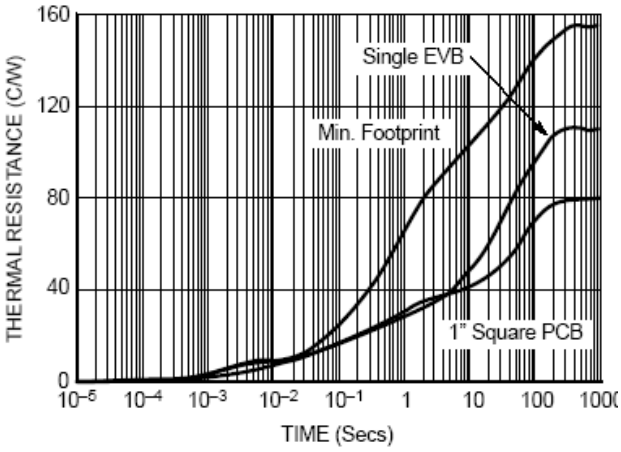

Figure 5. Single 1206A ChipFET

SUMMARY

The thermal results for the 1206A ChipFET package display similar power dissipation performance to the SO−8 with a footprint reduction of 80%.

Careful design of the package has allowed for this performance to be achieved. The short leads allow the die size to be maximized and thermal resistance to be reduced to provide a higher performance part compared to the TSOP−6 (SOT23−6).

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